Code No: P18ECT03

R18

HALL TICKET NUMBER

PACE INSTITUTE OF TECHNOLOGY & SCIENCES::ONGOLE
(AUTONOMOUS)
II B.TECH I SEMESTER END SUPPLEMENTARY EXAMINATIONS, MARCH/APRIL - 2023
SWITCHING THEORY AND LOGIC DESIGN
(ECE Branch)

Time: 3 hours Max. Marks: 60

Note: Question Paper consists of Two parts (Part-A and Part-B)

PART-A

Answer all the questions in Part-A (5X2=10M)

Q.No.		Questions	Marks	CO	KL
1	a)	Convert $(11010.11)_2$ into decimal.	[2M]	1	
	b)	What are don't cares?	[2M]	2	
	c)	List the applications of PAL and PLA.	[2M]	3	
	d)	Compare latch and flip-flop.	[2M]	4	
	e)	Distinguish between Moore and Mealy Machines.	[2M]	5	

PART-B

Answer One Question from each UNIT (5X10=50M)

Q.No.		Questions	Marks	CO	KL
		UNIT-I			
2.	a)	Represent the following numbers in decimal number system: (i) $(1010101)_2$ (ii) $(26.24)_8$	[5M]	1	
	b)	Implement the Boolean function: $F = xy + x'y' + y'z$ using with NOR and inverter gates.	[5M]	1	
		OR			
3.	a)	Represent +35 and -35 in sign magnitude, sign 1's complement and sign 2's complement representation.	[5M]	1	
	b)	Simplify the following Boolean function into (i) sum-of-products form and (ii) product-of-sums form: $F(A,B,C,D) = \sum(0,1,2,5,8,9,10)$	[5M]	1	
		UNIT-II			
4.	a)	Simplify the following Boolean functions, using *Karnaugh* maps: $F = A'B'C'D' + AC'D' + B'CD' + A'BCD + BC'D$	[5M]	2	
	b)	Draw and explain about half-adder and full-adder with neat sketches.	[5M]	2	
		OR			
5.	a)	Simplify the following Boolean functions using *Karnaugh* maps: $F(w,x,y,z) = \sum(0,1,2,4,5,6,8,9,12,13,14)$	[5M]	2	
	b)	Design and implement BCD to Excess-3 code converter.	[5M]	2	
		UNIT-III			
6.	a)	Using 8:1 multiplexer realize the Boolean function: T= f(w,x,y,z)= Σ(0,1,2,4,5,7,8,9,12,13)	[5M]	3	
	b)	Implement the following two Boolean functions with a PLA: $F_1(A,B,C) = \sum m(0,5,6,7)$; $F2(A,B,C) = \sum m(0,3,5,7)$	[5M]	3	
		OR			
7.	a)	With the help of a logic diagram and a truth table, explain a 3-line to 8-line decoder.	[5M]	3	
	b)	Briefly explain about PLDs.	[5M]	3	
		UNIT-IV			
8.	a)	Draw and explain about the D-Latch Flip-Flop and the clocked T Flip-Flop.	[5M]	4	

	b)	Convert SR flip-flop to JK flip-flop with an example.	[5M]	4	
		OR			
9.	a)	Write the differences between combinational and sequential circuits.	[5M]	4	
	b)	With neat sketches explain the JK flip-flop.	[5M]	4	
		UNIT-V			
10.	a)	Design and explain a 4-bit ring counter using D-flip flops with relevant timing diagrams.	[5M]	5	
	b)	A clocked sequential circuit with simple input X and single output Z produce an output Z = 1 whenever the input X completes the sequence 1 0 1 1 and overlapping is allowed. i) Obtain its state - diagram ii) Obtain its minimal state -table and design circuit with D- Flip-Flop	[5M]	5	
		OR			
11.	a)	Design a MOD-10 ripple counter.	[5M]	5	
	b)	With an example explain the procedure for conversion of Moore machine to Mealy machine.	[5M]	5	

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